Illinois Center for Wireless Systems

ICWS Seminar Series

Design of Low Power Digital Phase Lock Loops

Krishnaswamy Nagaraj
Texas Instruments

Wednesday, April 18, 2007, 11:00 am
B02 CSL

Abstact: With the trend towards system on chip integration, clock generation and distribution on a chip is an important problem. Present day SOC's use multiple phase lock loops (PLLs) for this purpose. With the trend towards digitally intensive technologies, digital phase lock loops (DPLLs) are now replacing the traditional analog phase lock loops (APLLs) in many applications. This talk will discuss the design of low power DPLLs.

Biography: Krishnaswamy Nagaraj has been with Texas Instruments since 1996. He is presently with the Wireless Terminal Business Unit. During 1986-1996, he was with the Bell Laboratories in Murray Hill, New Jersey. During 1985-1986 he was with the University of Waterloo in Canada. He has been engaged in the development of mixed-signal analog integrated circuits for application in Wireless and Wireline communications, data storage and signal processing.

He was an Associate Editor of the IEEE Transactions on Circuits and Systems, Part II, during 1993-1995, an Associate Editor of the IEEE Journal of Solid State Circuits, during 1998-2003 and is presently the Editor-in-Chief of the IEEE Journal of Solid State Circuits. He is a Fellow of the IEEE.

He has an Adjunct Associate Professor at the University of Pennsylvania since 1996.

ICWS Seminar series is supported by a grant from Rockwell Collins